LTC1658

14-Bit Rail-to-Rail Micropower DAC

September 1998

FEATURES

- 14-Bit Resolution
- **8-Lead MSOP Package**
- **Buffered True Rail-to-Rail Voltage Output**
- 3V or 5V Single Supply Operation
- Very Low Power: $I_{CC(TYP)}$ = 270µA
- Power-On Reset
- 3-Wire Cascadable Serial Interface is Compatible with SPI and MICROWIRE™
- **Maximum DNL Error: 1LSB**
- Low Cost

APPLICATIONS

- Digital Calibration
- Industrial Process Control
- Automatic Test Equipment
- Cellular Telephones

DESCRIPTION

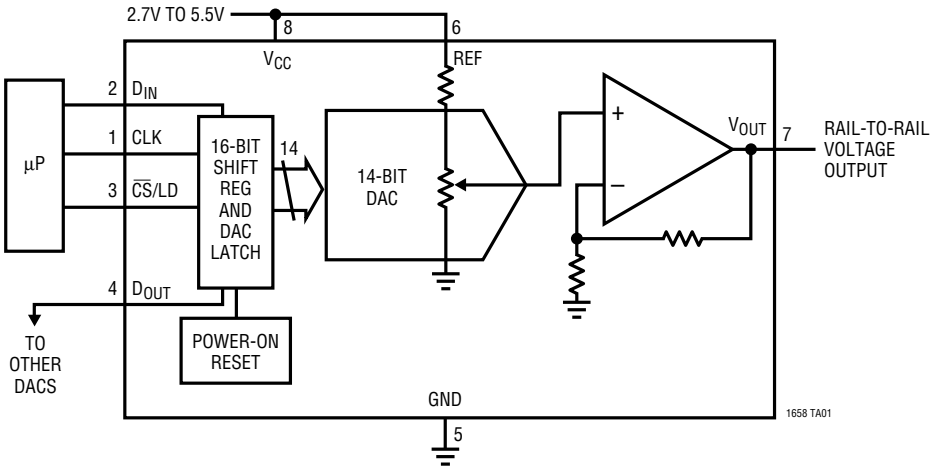
The LTC®1658 is a single supply, rail-to-rail voltage output, 14-bit digital-to-analog converter (DAC) in an 8-lead MSOP package. It includes an output buffer amplifier and an easy-to-use 3-wire cascadable serial interface.

The LTC1658 output swings from 0V to V_{REF}. The REF pin can be tied to V_{CC} for rail-to-rail output swing. The LTC1658 operates from a single 2.7V to 5.5V supply. The typical power supply current is 270µA.

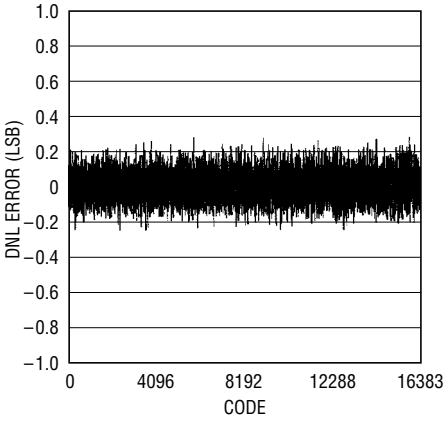
The low power supply current makes the LTC1658 ideal for battery-powered applications. The space saving MSOP provides the smallest 14-bit DAC system available.

TYPICAL APPLICATION

Functional Block Diagram: 14-Bit Rail-to-Rail DAC



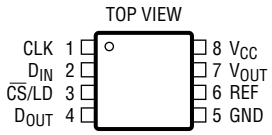
Differential Nonlinearity vs Input Code



ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND ..... –0.5V to 7.5V
TTL Input Voltage ..... –0.5V to 7.5V
V_{REF} .....–0.5V to 7.5V
V_{OUT} ..... –0.5V to V_{CC} + 0.5V
Junction Temperature ..... –65°C to 125°C
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

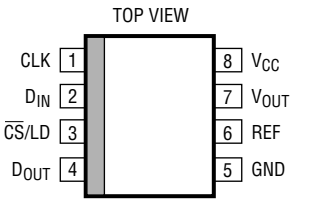
PACKAGE/ORDER INFORMATION



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 250°C/W

ORDER PART NUMBER
LTC1658CMS8 LTC1658IMS8
MS8 PART MARKING
LTCW LTFW



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 100°C/W(N8)
T_{JMAX} = 125°C, θ_{JA} = 150°C/W(S8)

ORDER PART NUMBER
LTC1658CN8 LTC1658IN8 LTC1658CS8 LTC1658IS8
S8 PART MARKING
1658 1658I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{CC} = 2.7V to 5.5V, V_{OUT} unloaded, REF ≤ V_{CC}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DAC							
	Resolution		●	14			Bits
	Monotonicity		●	14			Bits
DNL	Differential Nonlinearity	$V_{REF} \le V_{CC}$ – 0.1V (Note 1)	●			±1.0	LSB
INL	Integral Nonlinearity	$V_{REF} \le V_{CC}$ – 0.1V (Note 1)	●			±8.0	LSB
ZSE	Zero Scale Error		●	0		7	mV
V_{OS}	Offset Error	Measured at Code 50	●			±7	mV
V_{OS}TC	Offset Error Temperature Coefficient				±15		µV/°C
	Gain Error		●			±20	LSB
	Gain Error Drift				5		ppm/°C
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance	●	2.7		5.5	V
I_{CC}	Supply Current	2.7V ≤ V_{CC} ≤ 5.5V (Note 3)	●		270	550	µA
Op Amp DC Performance							
	Short-Circuit Current Low	V_{OUT} Shorted to GND	●		55	120	mA
	Short-Circuit Current High	V_{OUT} Shorted to V_{CC}	●		55	120	mA
	Output Impedance to GND	Input Code = 0	●		70	200	Ω
	Output Line Regulation	Input Code = 16383, V_{CC} = 2.7V to 5.5V, REF = 2.5V	●			1.5	mV/V

ELECTRICAL CHARACTERISTICS

V_{CC} = 2.7V to 5.5V, V_{OUT} unloaded, REF ≤ V_{CC}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
AC Performance							
	Voltage Output Slew Rate		●	0.35	1.0		V/µs
	Voltage Output Settling Time	(Note 2) to ±0.5LSB			12		µs
	Digital Feedthrough				0.3		nV•s
Reference Input							
R_{IN}	REF Input Resistance		●	30	60		kΩ
REF	REF Input Range	(Notes 4, 5)	●	0		V_{CC}	V
Digital I/O							
V_{IH}	Digital Input High Voltage	V_{CC} = 5V	●	2.4			V
V_{IL}	Digital Input Low Voltage	V_{CC} = 5V	●			0.8	V
V_{OH}	Digital Output High Voltage	V_{CC} = 5V, I_{OUT} = –1mA, D_{OUT} Only	●	V_{CC} – 0.7			V
V_{OL}	Digital Output Low Voltage	V_{CC} = 5V, I_{OUT} = 1mA, D_{OUT} Only	●			0.4	V
V_{IH}	Digital Input High Voltage	V_{CC} = 3V	●	2.0			V
V_{IL}	Digital Input Low Voltage	V_{CC} = 3V	●			0.6	V
V_{OH}	Digital Output High Voltage	V_{CC} = 3V, I_{OUT} = –1mA, D_{OUT} Only	●	V_{CC} – 0.7			V
V_{OL}	Digital Output Low Voltage	V_{CC} = 3V, I_{OUT} = 1mA, D_{OUT} Only	●			0.4	V
I_{LEAK}	Digital Input Leakage	V_{IN} = GND to V_{CC}	●			±10	µA
C_{IN}	Digital Input Capacitance	(Note 5)	●			10	pF
Switching (V_{CC} = 4.5V to 5.5V)							
t_1	D_{IN} Valid to CLK Setup		●	40			ns
t_2	D_{IN} Valid to CLK Hold		●	0			ns
t_3	CLK High Time	(Note 5)	●	40			ns
t_4	CLK Low Time	(Note 5)	●	40			ns
t_5	$\overline{CS}$/LD Pulse Width	(Note 5)	●	50			ns
t_6	LSB CLK to $\overline{CS}$/LD	(Note 5)	●	40			ns
t_7	$\overline{CS}$/LD Low to CLK	(Note 5)	●	20			ns
t_8	D_{OUT} Output Delay	C_{LOAD} = 15pF	●	5		100	ns
t_9	CLK Low to $\overline{CS}$/LD Low	(Note 5)	●	20			ns
Switching (V_{CC} = 2.7V to 5.5V)							
t_1	D_{IN} Valid to CLK Setup		●	60			ns
t_2	D_{IN} Valid to CLK Hold		●	0			ns
t_3	CLK High Time	(Note 5)	●	60			ns
t_4	CLK Low Time	(Note 5)	●	60			ns
t_5	$\overline{CS}$/LD Pulse Width	(Note 5)	●	80			ns
t_6	LSB CLK to $\overline{CS}$/LD	(Note 5)	●	60			ns
t_7	$\overline{CS}$/LD Low to CLK	(Note 5)	●	30			ns
t_8	D_{OUT} Output Delay	C_{LOAD} = 15pF	●	10		150	ns
t_9	CLK Low to $\overline{CS}$/LD Low	(Note 5)	●	30			ns

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Nonlinearity is defined from code 50 to code 16383 (full scale). See Applications Information.

Note 2: DAC switched between all 1s and code 50.

Note 3: Digital inputs at 0V or V_{CC}.

Note 4: V_{OUT} can only swing from (GND + $|V_{OS}|$) to (V_{CC} – $|V_{OS}|$) when output is unloaded.

Note 5: Guaranteed by design. Not subject to test.

PIN FUNCTIONS

CLK (Pin 1): The TTL Level Input for the Serial Interface Clock.

D_{IN} (Pin 2): The TTL Level Input for the Serial Interface Data. Data on the D_{IN} pin is latched into the shift register on the rising edge of the serial clock and is loaded MSB first. The LTC1658 requires a 16-bit word to be loaded in. The last two bits are don't cares.

$\overline{CS}$/LD (Pin 3): The TTL Level Input for the Serial Interface Enable and Load Control. When $\overline{CS}$/LD is low the CLK signal is enabled, so the data can be clocked in. When $\overline{CS}$/LD is pulled high, data is loaded from the shift register into the DAC register, updating the DAC output.

D_{OUT} (Pin 4): Output of the Shift Register Which Becomes Valid on the Rising Edge of the Serial Clock.

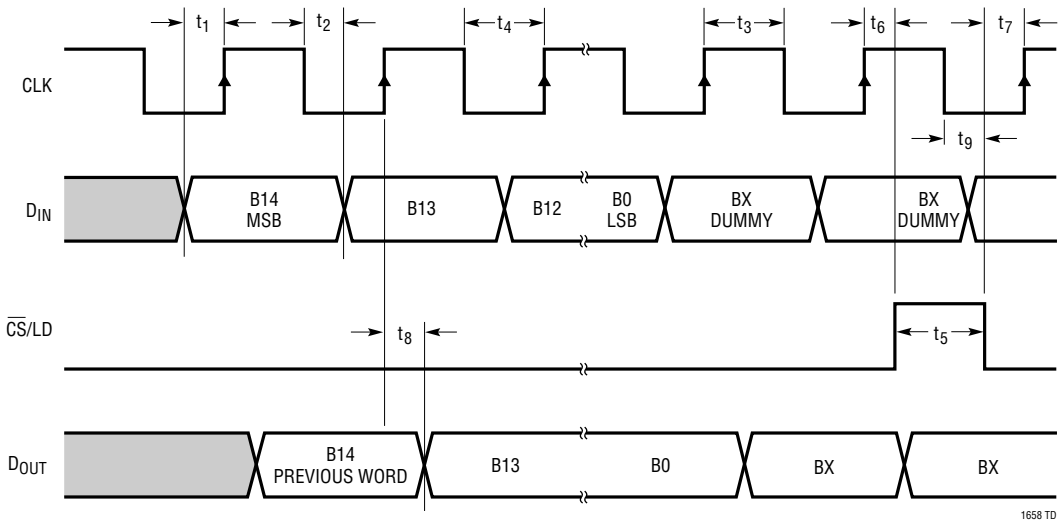
GND (Pin 5): Ground.

REF (Pin 6): Reference Input. There is a gain of one from this pin to the output. When tied to V_{CC} the output will swing from GND to V_{CC}. The output can only swing to within it's offset specification to V_{CC} (see Applicatons Information).

V_{OUT} (Pin 7): Buffered Rail-to-Rail DAC Output.

V_{CC} (Pin 8): Positive Supply Input. 2.7V ≤ V_{CC} ≤ 5.5V.

TIMING DIAGRAM



DEFINITIONS

Differential Nonlinearity (DNL): The difference between the measured change and the ideal 1LSB change for any two adjacent codes. The DNL error between any two codes is calculated as follows:

$$DNL = (\Delta V_{OUT} - LSB)/LSB$$

Where ΔV_{OUT} is the measured voltage difference between two adjacent codes.

Digital Feedthrough: The glitch that appears at the analog output caused by AC coupling from the digital inputs when they change state. The area of the glitch is specified in (nV)(sec).

Gain Error: Gain error is the difference between the output of a DAC from its ideal full-scale value after offset error has been adjusted.

Integral Nonlinearity (INL): The deviation from a straight line passing through the endpoints of the DAC transfer curve (Endpoint INL). Because the output cannot go below zero, the linearity is measured between full scale and the lowest code which guarantees the output will be greater than zero. The INL error at a given input code is calculated as follows:

$$INL = [V_{OUT} - V_{OS} - (V_{FS} - V_{OS})(code/16383)]/LSB$$

Where V_{OUT} is the output voltage of the DAC measured at the given input code.

Least Significant Bit (LSB): The ideal voltage difference between two successive codes.

$$LSB = V_{REF}/16384$$

Resolution (n): Defines the number of DAC output states (2^n) that divide the full-scale range. Resolution does not imply linearity.

Voltage Offset Error (V_{OS}): Nominally, the voltage at the output when the DAC is loaded with all zeros. A single supply DAC can have a true negative offset, but the output cannot go below zero (see Applications Information).

For this reason, single supply DAC offset is measured at the lowest code that guarantees the output will be greater than zero.

OPERATION

Serial Interface

The data on the D_{IN} input is loaded into the shift register on the rising edge of the clock. The MSB is loaded first. The DAC register loads the data from the shift register when $\overline{CS}$/LD is pulled high. The clock is disabled internally when $\overline{CS}$/LD is high. Note: CLK must be low before $\overline{CS}$/LD is pulled low to avoid an extra internal clock pulse. The input word must be 16 bits wide. The last two bits are don't cares.

The buffered output of the 16-bit shift register is available on the D_{OUT} pin which swings from GND to V_{CC}.

Multiple LTC1658s may be daisy-chained together by connecting the D_{OUT} pin to the D_{IN} pin of the next chip while the clock and $\overline{CS}$/LD signals remain common to all chips in the daisy chain. The serial data is clocked to all of the chips then the $\overline{CS}$/LD signal is pulled high to update all of them simultaneously.

Voltage Output

The LTC1658 rail-to-rail buffered output can source or sink 5mA over the entire operating temperature range while pulling to within 300mV of the positive supply voltage or ground. The output swings to within a few millivolts of either supply rail when unloaded and has an equivalent output resistance of 40Ω when driving a load to the rails. The output can drive 1000pF without going into oscillation.

The output swings from 0V to the voltage at the REF pin, i.e., there is a gain of 1 from the REF to V_{OUT}. Please note, if REF is tied to V_{CC} the output can only swing to ($V_{CC} - V_{OS}$). See Applications Information.

APPLICATIONS INFORMATION

Rail-to-Rail Output Considerations

In any rail-to-rail DAC, the output swing is limited to voltages within the supply range.

If the DAC offset is negative, the output for the lowest codes limits at 0V as shown in Figure 1b.

Similarly, limiting can occur near full scale when the REF pin is tied to V_{CC}. If $V_{REF} = V_{CC}$ and the DAC full-scale error (FSE) is positive, the output for the highest codes limits at V_{CC} as shown in Figure 1c. No full-scale limiting can occur if V_{REF} is less than V_{CC} – FSE.

Offset and linearity are defined and tested over the region of the DAC transfer function where no output limiting can occur.

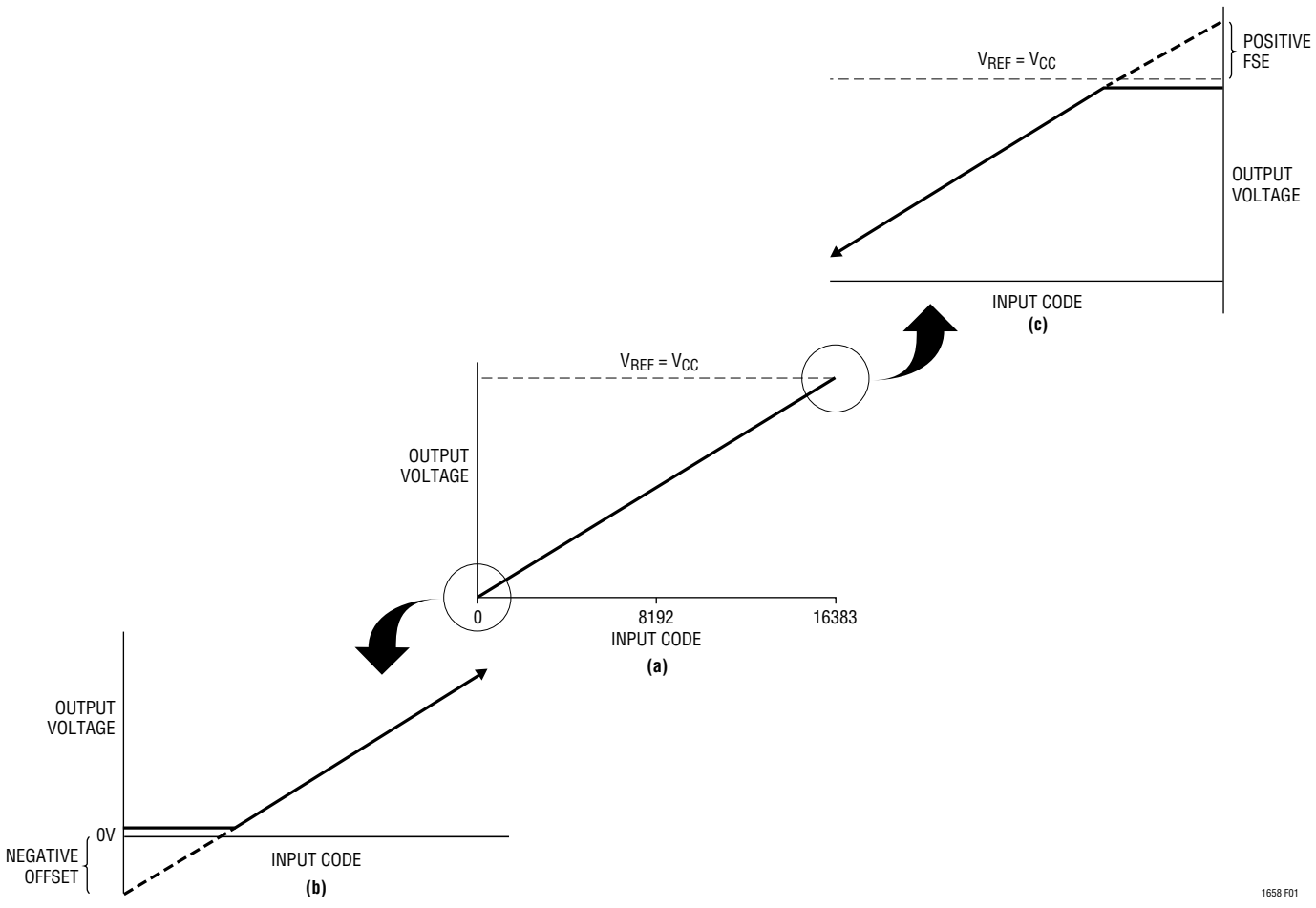
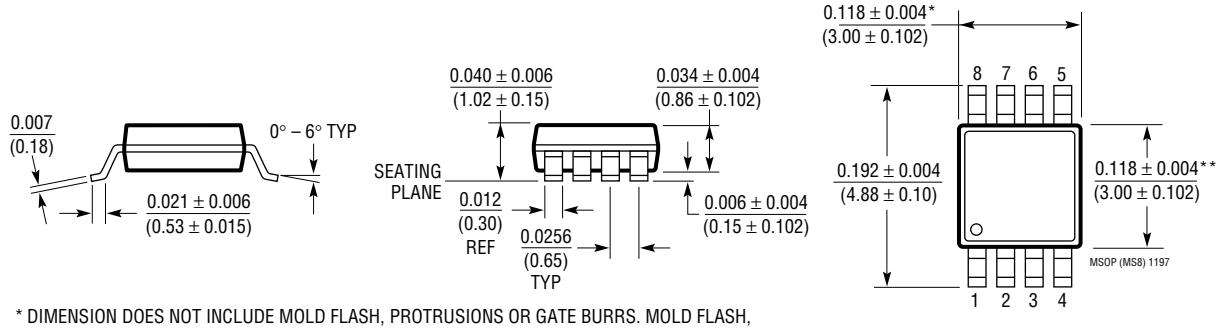


Figure 1. Effects of Rail-to-Rail Operation On a DAC Transfer Curve. (a) Overall Transfer Function (b) Effect of Negative Offset for Codes Near Zero Scale (c) Effect of Positive Full-Scale Error for Input Codes Near Full Scale When $V_{REF} = V_{CC}$

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

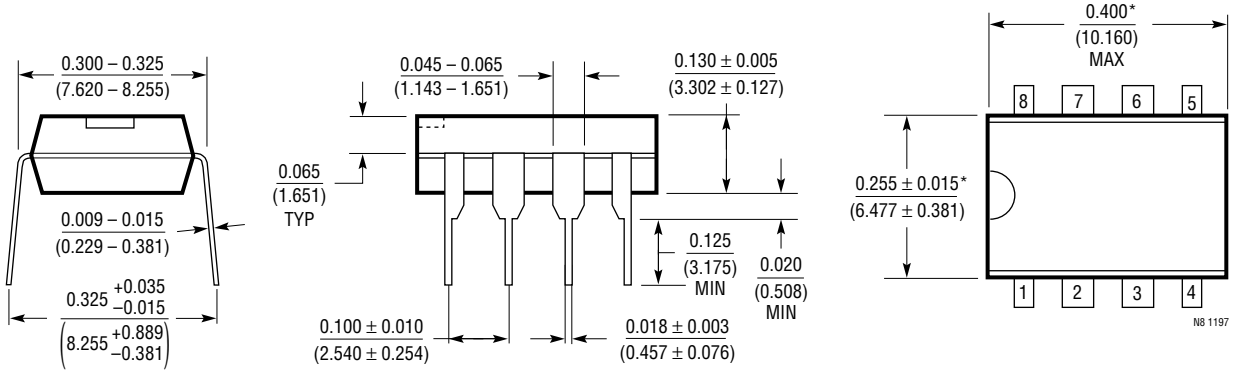
MS8 Package
8-Lead Plastic MSOP
(LTC DWG # 05-08-1660)



* DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

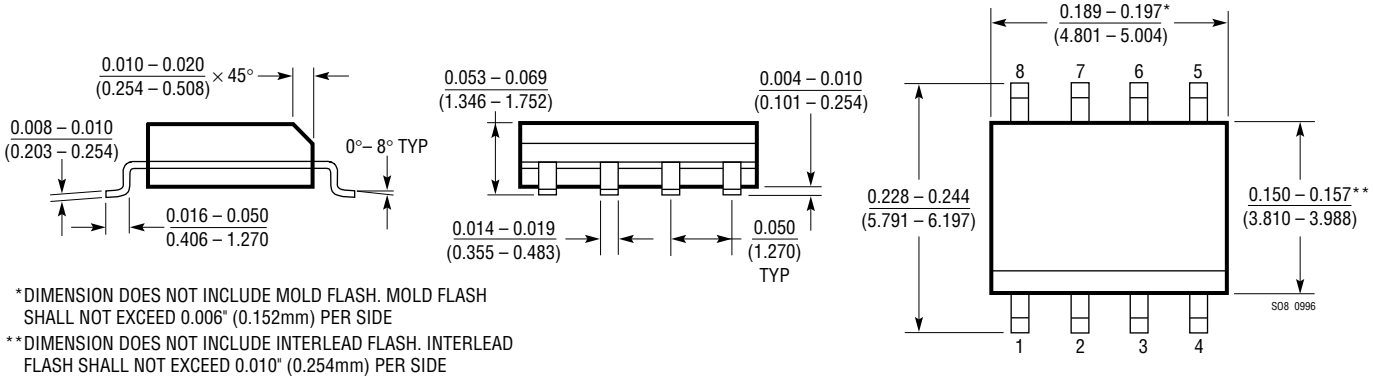
** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)

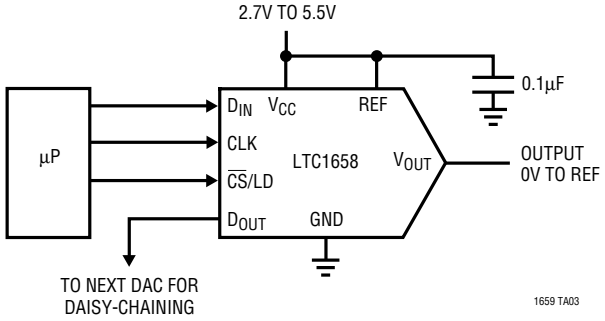


*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

14-Bit, 3V to 5V Single Supply, Voltage Output DAC



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1257	Single 12-Bit V_{OUT} DAC, Full Scale: 2.048V, V_{CC}: 4.75V to 15.75V, Reference Can Be Overdriven Up to 12V, i.e., FS_{MAX} = 12V	5V to 15V Single Supply, Complete V_{OUT} DAC in SO-8 Package
LTC1446/LTC1446L	Dual 12-Bit V_{OUT} DACs in SO-8 Package	LTC1446: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.095V LTC1446L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1448	Dual 12-Bit V_{OUT} DAC, V_{CC}: 2.7V to 5.5V	Output Swings from GND to REF. REF Input Can Be Tied to V_{CC}
LTC1450/LTC1450L	Single 12-Bit V_{OUT} DACs with Parallel Interface	LTC1450: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.095V LTC1450L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1451	Single Rail-to-Rail 12-Bit DAC, Full Scale: 4.095V, V_{CC}: 4.5V to 5.5V, Internal 2.048V Reference Brought Out to Pin	5V, Low Power Complete V_{OUT} DAC in SO-8 Package
LTC1452	Single Rail-to-Rail 12-Bit V_{OUT} Multiplying DAC, V_{CC}: 2.7V to 5.5V	Low Power, Multiplying V_{OUT} DAC with Rail-to-Rail Buffer Amplifier in SO-8 Package
LTC1453	Single Rail-to-Rail 12-Bit V_{OUT} DAC, Full Scale: 2.5V, V_{CC}: 2.7V to 5.5V	3V, Low Power, Complete V_{OUT} DAC in SO-8 Package
LTC1454/LTC1454L	Dual 12-Bit V_{OUT} DACs in SO-16 Package with Added Functionality	LTC1454: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.095V LTC1454L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1456	Single Rail-to-Rail Output 12-Bit DAC with Clear Pin, Full Scale: 4.095V, V_{CC}: 4.5V to 5.5V	Low Power, Complete V_{OUT} DAC in SO-8 Package with Clear Pin
LTC1458/LTC1458L	Quad 12 Bit Rail-to-Rail Output DACs with Added Functionality	LTC1458: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.095V LTC1458L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1659	Single Rail-to-Rail 12-Bit V_{OUT} DAC in 8-Pin MSOP, V_{CC} = 2.7V to 5.5V	Low Power, Multiplying V_{OUT} DAC in MS8 Package. Output Swings from GND to REF. REF Input Can Be Tied to V_{CC}.

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